CLAIMS

1. An apparatus defined to communicate electronically with each of a Serial Attached SCSI (SAS) protocol device and a Serial ATA (SATA) protocol device, comprising:

a phy configured to connect the apparatus to each of the SAS protocol device and the SATA protocol device;

wired endian logic configured to communicate through the phy, the wired endian logic configured to interface a wired endian format of the apparatus with each of a big endian format of the SAS protocol device and a little endian format of the SATA protocol device; and

internal circuitry configured to operate in accordance with the wired endian format.

2. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 1, wherein the internal circuitry configured to operate in accordance with the wired endian format is defined to store and process a sequence of bytes in transmit order.

3. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 2, wherein the sequence of bytes is represented as a sequence of four bytes being stored in consecutive memory locations, the transmit order defined to begin with a lowest memory address associated with the sequence of bytes and progress consecutively through the remaining memory addresses associated with the sequence of bytes.

4. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 1, wherein the wired endian logic includes transmission logic including,

discrimination circuitry defined to identify a sequence of bytes in wired endian format as one of a control sequence of bytes and a data sequence of bytes,

data sequence processing circuitry defined to convert the data sequence of bytes from the wired endian format to a native format associated with a device to which the data sequence of bytes is to be transmitted, the data sequence processing circuitry also being defined to perform pre-transmission processing on the data sequence of bytes while in native format, the data sequence processing circuitry being further defined to convert the data sequence of bytes from the native format back to the wired endian format upon completion of pre-transmission processing, and

transmission circuitry defined to transmit the sequence of bytes in wired endian format.

5. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 4, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive.

6. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 4, wherein the data sequence processing circuitry is defined to represent the native format as the big endian format for the SAS protocol device and the little endian format for the SATA protocol device.

7. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 4, wherein the pre-transmission processing includes cyclic redundancy check data generation and scrambling of the data sequence of bytes.

8. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 1, wherein the wired endian logic includes receipt logic including,

receiving circuitry defined to receive a sequence of bytes in a native format associated with a device from which the data sequence of bytes is to have been transmitted,

discrimination circuitry defined to identify the sequence of bytes in native format as one of a control sequence of bytes and a data sequence of bytes,

data sequence processing circuitry defined to perform receipt processing on the data sequence of bytes while in native format, the receipt processing including unscrambling of the data sequence of bytes and cyclic redundancy check data generation, and

conversion circuitry defined to convert the sequence of bytes from the native format to the wired endian format.

9. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 8, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive.

10. An apparatus defined to communicate electronically with each of a SAS protocol device and a SATA protocol device as recited in claim 8, wherein the receiving circuitry is defined to represent the native format as the big endian format for the SAS protocol device and the little endian format for the SATA protocol device.

11. A method for operating a wired endian device to perform a transmission operation, comprising:

identifying a sequence of bytes to be transmitted as one of a control sequence of bytes and a data sequence of bytes, the sequence of bytes to be transmitted being maintained in a wired endian format;

converting the sequence of bytes having been identified as the data sequence of bytes from the wired endian format to a native format, wherein the native format is associated with a device to which the sequence of bytes is to be transmitted;

processing the data sequence of bytes in the native format, wherein the processing includes generating cyclic redundancy check data and scrambling the data sequence of bytes;

converting the data sequence of bytes from the native format to the wired endian format; and

transmitting the sequence of bytes in accordance with the wired endian format.

12. A method for operating a wired endian device to perform a transmission operation as recited in claim 11, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive.

13. A method for operating a wired endian device to perform a transmission operation as recited in claim 11, wherein the wired endian format includes storage and transmission of the sequence of bytes in transmit order.

14. A method for operating a wired endian device to perform a transmission operation as recited in claim 13, wherein the sequence of bytes is represented as a sequence of four bytes being stored in consecutive memory locations, the transmit order defined to begin with a lowest memory address associated with the sequence of bytes and progress consecutively through the remaining memory addresses associated with the sequence of bytes.

15. A method for operating a wired endian device to perform a transmission operation as recited in claim 11, wherein the native format is represented as a big endian format when the device to which the sequence of bytes is to be transmitted is a Serial Attached SCSI (SAS) device, and the native format being represented as a little endian format when the device to which the sequence of bytes is to be transmitted is a Serial ATA (SATA) device.

16. A method for operating a wired endian device to receive a transmission, comprising:

receiving a sequence of bytes in a native format, wherein the native format is associated with a device from which the sequence of bytes was transmitted;

identifying the sequence of bytes in the native format as representing one of a control sequence of bytes and a data sequence of bytes;

processing the data sequence of bytes in the native format, wherein the processing includes unscrambling the data sequence of bytes and generating cyclic redundancy check data; and

converting the sequence of bytes from the native format to a wired endian format.

17. A method for operating a wired endian device to receive a transmission as recited in claim 16, wherein the control sequence of bytes represents one of a Serial Attached SCSI (SAS) primitive and a Serial ATA (SATA) primitive.

18. A method for operating a wired endian device to receive a transmission as recited in claim 16, wherein the wired endian format includes storage and transmission of the sequence of bytes in transmit order.

19. A method for operating a wired endian device to receive a transmission as recited in claim 18, wherein the sequence of bytes is represented as a sequence of four bytes being stored in consecutive memory locations, the transmit order defined to begin with a lowest memory address associated with the sequence of bytes and progress consecutively through the remaining memory addresses associated with the sequence of bytes.

20. A method for operating a wired endian device to receive a transmission as recited in claim 16, wherein the native format is represented as a big endian format when the device from which the sequence of bytes was transmitted is a Serial Attached SCSI (SAS) device, and the native format being represented as a little endian format when the device from which the sequence of bytes was transmitted is a Serial ATA (SATA) device.